

-19-

WHAT IS CLAIMED IS:

1. A flip chip substrate comprising:
 - a plurality of conductive layers, including a top layer and a bottom layer;
 - a first plurality of contacts, including first and second contacts corresponding to a differential signal pair, which are arranged on the top layer within a die bonding area;
 - a second plurality of contacts, including third and fourth contacts corresponding to the differential signal pair, which are arranged on the bottom layer; and
 - first and second traces routed between the first and third contacts and between the second and fourth contacts, respectively, wherein the second trace is routed out of the die bonding area on a different one of the layers than the first trace and comprises a via in the die bonding area extending from the top layer to another of the plurality of layers, wherein the via is laterally offset from the second contact in a direction toward the first contact.
2. The flip chip substrate of claim 1 wherein:
 - the first trace is routed outwardly from the first contact toward an edge of the die bonding area along the top layer; and

-20-

the second trace is routed from the second contact to the different layer and outwardly toward the edge of the die bonding area along the different layer.

3. The flip chip substrate of claim 2 wherein the edge of the die bonding area is a nearest edge of the die bonding area to the first and second contacts.

4. The flip chip substrate of claim 2 wherein the different layer comprises the bottom layer, which is non-adjacent to the top layer.

5. The flip chip substrate of claim 2 wherein the different layer is disposed between the top layer and the bottom layer.

6. The flip chip substrate of claim 5 wherein the different layer is immediately adjacent to the top layer.

7. The flip chip substrate of claim 2 wherein:
the second trace is routed from the different layer back up to the top layer externally to the die bonding area; and
the first and second traces extend along the top layer outside of the die bonding area to respective vias located externally to the die bonding area and are routed downwardly

-21-

from the respective vias toward the third and fourth contacts, respectively.

8. The flip chip substrate of claim 7 wherein the respective vias are located in a region on the top layer that is generally vertical of the third and fourth contacts.

9. The flip chip substrate of claim 1 wherein the first and second contacts form a pair of adjacent signal contacts in the die bonding area.

10. The flip chip substrate of claim 1 wherein the third and fourth contacts form a pair of adjacent signal contacts on the bottom layer, external to the die bonding area.

11. The flip chip substrate of claim 1 wherein the second contact is located further from a nearest edge of the die bonding region than the first contact.

12. The flip chip substrate of claim 1 wherein:
the third and fourth contacts are adjacent to one another on the bottom layer; and
the first and second traces comprise respective vias extending from the bottom layer to another of the plurality of layers, wherein the respective vias are laterally offset toward one another relative to centers of

-22-

the third and fourth contacts, respectively.

13. A flip chip substrate comprising:
- a plurality of conductive layers, including a top layer and a bottom layer;
 - a first plurality of contacts, including first and second contacts corresponding to a differential signal pair, which are arranged on the top layer within a die bonding area;
 - a second plurality of contacts, including third and fourth contacts corresponding to the differential signal pair, which are arranged on the bottom layer;
 - a first trace electrically connecting the first and third contacts and having a first segment extending outwardly from the first contact toward an edge of the die bonding area along the top layer; and
 - a second trace electrically connecting the second and fourth contacts, wherein the second trace extends from the second contact to a second one of the layers within the die bonding area, which is located between the top and bottom layers, extends outwardly from the die bonding area along the second layer, and returns to the top layer externally to the die bonding area, and

-23-

wherein the first and second traces extend along the top layer outside of the die bonding area to respective vias and extend downwardly from the respective vias toward the third and fourth contacts, respectively.

14. The flip chip substrate of claim 13 wherein the second trace comprises a further via extending from the top layer to the second layer within the die bonding area and wherein the further via is laterally offset from a center of the second contact in a direction toward the first contact.

15. The flip chip substrate of claim 13 wherein the first and second traces are routed outwardly along the top and second layers, respectively, toward a nearest edge of the die bonding area to the first and second contacts.

16. The flip chip substrate of claim 13 wherein the second layer is immediately adjacent to the top layer.

17. The flip chip substrate of claim 13 wherein the respective vias are located adjacent to one another in a region on the top layer that is generally vertical of the third and fourth contacts.

-24-

18. The flip chip substrate of claim 13 wherein the first and second contacts form a pair of adjacent signal contacts in the die bonding area.

19. The flip chip substrate of claim 13 wherein the third and fourth contacts form a pair of adjacent signal contacts on the bottom layer, external to the die bonding area.

20. The flip chip substrate of claim 13 wherein the second contact is located further from a nearest edge of the die bonding region than the first contact.

21. The flip chip substrate of claim 13 wherein:
the third and fourth contacts are adjacent to one another on the bottom layer; and
the first and second traces comprise a second pair of respective vias extending from the bottom layer to another of the plurality of layers, wherein the second pair of respective vias are laterally offset toward one another relative to centers of the third and fourth contacts, respectively.

22. A flip chip substrate comprising:
a plurality of conductive layers, including a top layer and a bottom layer;
a first plurality of contacts, including first and second contacts corresponding to a

-25-

differential signal pair, which are arranged on the top layer within a die bonding area;

a second plurality of contacts, including third and fourth adjacent contacts corresponding to the differential signal pair, which are arranged on the bottom layer; and

first and second traces routed between the first and third contacts and between the second and fourth contacts, respectively, the first and second traces comprising a pair of respective vias extending from the bottom layer to another of the plurality of layers, wherein the pair of respective vias are laterally offset toward one another relative to centers of the third and fourth contacts, respectively.

23. The flip chip substrate of claim 22 wherein:

the second trace is routed out of the die bonding area on a different one of the layers than the first trace and comprises a via in the die bonding area extending from the top layer to another of the plurality of layers, and wherein the via is laterally offset from the second contact in a direction toward the first contact.

24. The flip chip substrate of claim 23 wherein:

-26-

the first trace is routed outwardly from the first contact toward an edge of the die bonding area along the top layer; and
the second trace is routed from the second contact to the different layer and outwardly toward the edge of the die bonding area along the different layer.

25. The flip chip substrate of claim 23 wherein the edge of the die bonding area is a nearest edge of the die bonding area to the first and second contacts.

26. The flip chip substrate of claim 23 wherein the different layer comprises the bottom layer, which is non-adjacent to the top layer.

27. The flip chip substrate of claim 23 wherein the different layer is disposed between the top layer and the bottom layer.

28. The flip chip substrate of claim 27 wherein the different layer is immediately adjacent to the top layer.

29. The flip chip substrate of claim 23 wherein:
the second trace is routed from the different layer back up to the top layer externally to the die bonding area; and

-27-

the first and second traces extend along the top layer outside of the die bonding area to a second pair of respective vias located externally to the die bonding area and are routed downwardly from the second pair of respective vias toward the first pair of respective vias, respectively.

30. The flip chip substrate of claim 29 wherein the second pair of respective vias are located in a region on the top layer that is generally vertical of the third and fourth contacts and the first pair of respective vias.

31. The flip chip substrate of claim 22 wherein the first and second contacts form a pair of adjacent signal contacts in the die bonding area.

32. The flip chip substrate of claim 22 wherein the second contact is located further from a nearest edge of the die bonding region than the first contact.